

**IN THE ABSTRACT**

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**ABSTRACT**

A memory cell comprises one MOS transistor having a floating bulk region which is electrically isolated from others. A gate electrode of the MOS transistor is connected to a word line, a drain diffusion region thereof is connected to a bit line, and a source diffusion region thereof is connected to a fixed potential line. The memory cell stores a first threshold state in which majority carriers produced by impact ionization are injected and held in the bulk region of the transistor and a second threshold state in which the majority carriers in the bulk region of the transistor are emitted by a forward bias at a pn junction on the drain side as binary data. Thereby, a semiconductor memory device uses a simple transistor structure memory cell, enabling dynamic storage of binary data by a small number of signal lines can be provided.